TGEN6320 Product Brief

1. Description

The TGEN6320 is a single-chip, PCIe Gen6 clock synthesizer. Crafted to operate as either a comprehensive clock solution or alongside DB2000Q/CK440Q ① -compliant clock buffers, it seamlessly delivers point-to-point clocks to numerous receiving agents. As a key component of the forthcoming clock generator lineage, this device offers robust compatibility with contemporary dual and multi-socket Intel server platforms.

NOTE: ① TGEN6320 doesn't support the Platform Time (PFT) Phase/Frequency Tracking function.

2. Features

- PCIe Clocking Architectures
  - Common Clocked (CC)
  - Independent Reference (IR) with and without spread spectrum
- PCIe Gen5 CC Phase Jitter < 40fs rms
- PCIe Gen6 CC Phase Jitter < 25fs rms
- 3.3V operation
- Side-Band Interface allows real-time hardware control of all output enables
- OE# pin control of 100M[6:0] supports PCIe slot CLKREQ#
- 85Ω differential Low-Power HCSL (LP-HCSL) outputs eliminate 80 resistors, saving 130mm2 of area
- 9 selectable SMBus addresses
- Supports 0%, -0.3% and -0.5% spread-spectrum amounts
- Three 25MHz output pairs
- Seven 100MHz output pairs with individual OE# pins
- Nine MXCLK output pairs multiplexable between 100MHz and 25MHz
- 8 × 8 mm dual-row QFN-100

3. Typical Applications

- Data Center
- X86/Arm Server
- Multi-function printer
- Wireless access point

TGEN6320 Product Brief

4. Functional Diagram

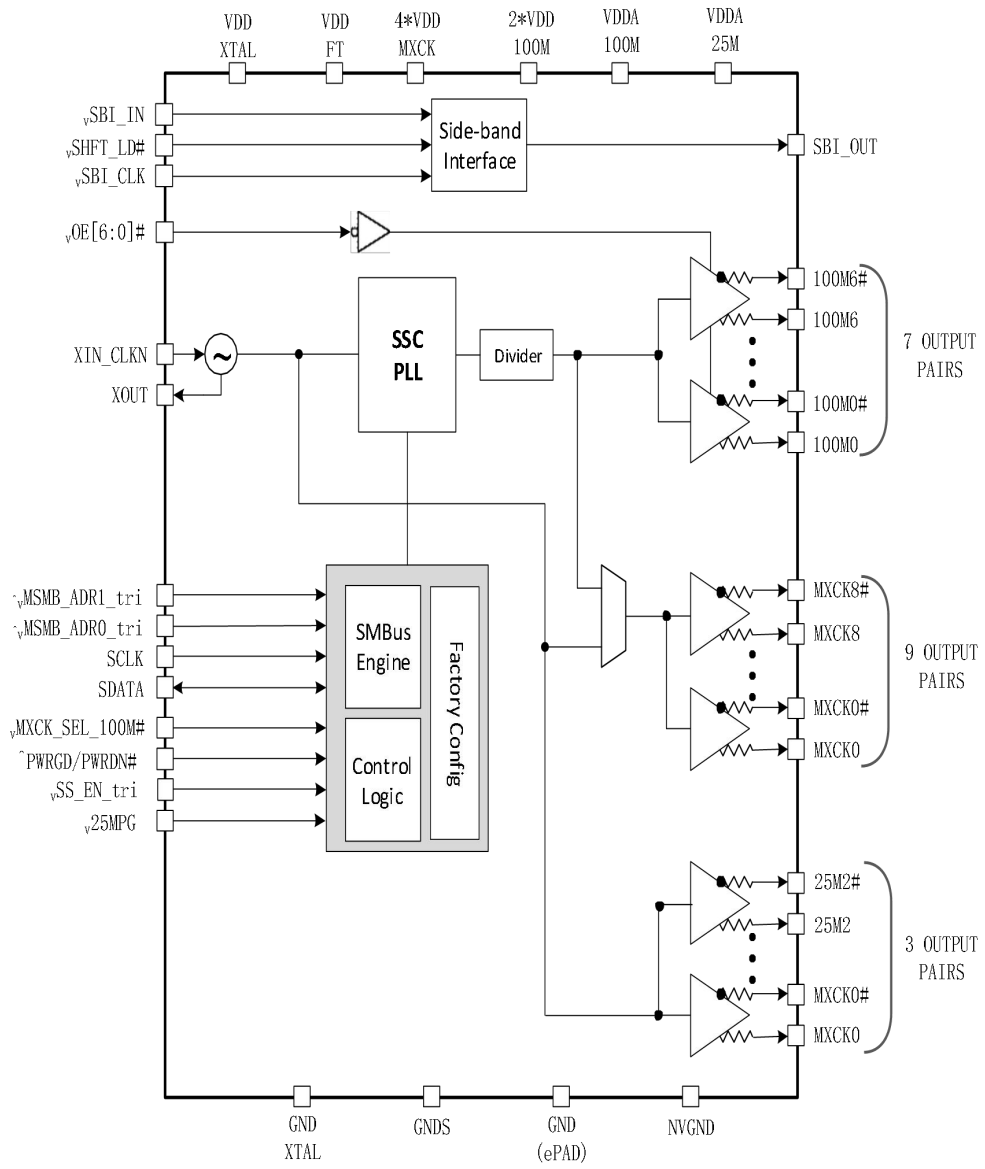

Figure 1 Functional Diagram

Note:

a) Pins with ^ prefix have internal pull-up resistor.
b) Pins with v prefix have internal pull-down resistor.
c) Pins with ^v prefix have internal